**III.** Solution. Three forces act at the node: a tension force directed to the left, a tension force directed to the right, and a downward gravitational force. Since the system is in equilibrium, the sum of the projections of all forces along each axis must be equal to zero. By resolving the forces into horizontal and vertical components and applying equilibrium conditions, the unknown force is determined using trigonometric relationships.

$$-T_A \cdot \sin\alpha + T_B \cdot \sin\beta = 0, \quad T_A = G_2 \qquad T_B = G_3$$

$$G_2 \cdot \sin\alpha = G_3 \cdot \sin\beta \qquad G_3 = \frac{G_2 \sin\alpha}{\sin\beta}$$

$$G_3 = \frac{G_2 \sin\alpha}{\sin\beta} = \frac{55 * \sin(75^0)}{\sin(60^0)} \approx 61.34N$$

Answer: (as obtained from calculations) $G_3 \approx 61.34N$

In this problem, the equilibrium of a system of forces transmitted through pulleys is analyzed. The forces acting at the node are resolved into horizontal and vertical components, and equilibrium conditions are applied. The results show that the equilibrium depends directly on the directions and angles of the ropes. By correctly analyzing these parameters, unknown quantities can be accurately determined.

**Conclusion.** Three main methods are used to analyze a system of intersecting forces at a point:

•the geometric method;

•the graphical method;

•the analytical method.

In practice, the most effective approach is the analytical method, which is based on resolving forces into components using trigonometric functions. Such systems are widely encountered in building structures, mechanical devices, lifting systems, and various engineering applications. A clear understanding of systems of intersecting forces provides a solid foundation for studying more advanced topics in mechanics. It helps explain the interaction of forces, the laws of equilibrium, and the nature of physical processes in a deeper and more systematic way.

**References:**


(1). Rashidov T.R., Shoziyotov Sh., Mamatqulov Sh. Nazariy mexanika asoslari. Toshkent, "O‘qituvchi", 1990.

(2). Xalilov A.J. Nazariy mexanika: Statika. Toshkent, "Voris-nashriyot", 2012.

(3). Mirsaidov M.M., Tojiyev R.J. Nazariy mexanikadan masalalar to‘plami. Toshkent, "O‘zbekiston", 2002.

(4). Hibbeler Russell C. Engineering Mechanics: Statics. 14th ed. Pearson Education, 2016.

(5). Beer Ferdinand P., Johnston E. Russell. Vector Mechanics for Engineers: Statics. McGraw-Hill, 2015.

(6). Meriam J.L., Kraige L.G. Engineering Mechanics: Statics. Wiley, 2018.

(7). Timoshenko Stephen P. Engineering Mechanics. McGraw-Hill, 1953.

(8). Boresi Arthur P., Schmidt Richard J. Engineering Mechanics: Statics. Brooks/Cole, 2003.

(9). Gere James M. Mechanics of Materials. Cengage Learning, 2012.



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## INFLUENCE OF AN INTERFACIAL $SiO_2$ LAYER ON CHARGE TRAPPING AND LEAKAGE CURRENT IN SEMICONDUCTOR–DIELECTRIC STRUCTURES


***Annotation.*** *The continuous scaling of semiconductor devices requires the use of materials with high dielectric permittivity. In this regard, titanium dioxide ($TiO_2$), due to its high dielectric constant, is considered a promising material for metal–dielectric–semiconductor (MDS) structures. However, the direct contact of the $TiO_2$ layer with the silicon substrate leads to an increase in the density of interface states, an increase in leakage current, and the appearance of hysteresis in capacitance–voltage (C–V) characteristics. In this work, the improvement of interface quality by introducing a thin silicon dioxide ($SiO_2$) interfacial layer between the silicon substrate and the $TiO_2$ dielectric layer is considered. Within the*

*proposed $Si/SiO_2/TiO_2$/metal structure, the effect of the interfacial layer on the density of charge trapping centers ($D_{it}$), leakage current, and electrophysical properties is analyzed theoretically.*

***Keywords.*** *MOS capacitor, titanium dioxide ($TiO_2$), silicon dioxide ($SiO_2$), interfacial layer, interface states, charge trapping centers, leakage current, capacitance–voltage characteristics, hysteresis, dielectric layer.*

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## $SiO_2$ ORALIQ QATLAMINING YARIMO'TKAZGICH–DIELEKTRIK TUZILMALARDA ZARYAD TUTILISHI VA OQISH TOKIGA TA'SIRI

***Annotatsiya.*** *Yarimo'tkazgich asboblarning uzluksiz kichrayib borishi yuqori dielektrik singdiruvchanlikka ega materiallardan foydalanishni talab qiladi. Shu munosabat bilan titan dioksid ($TiO_2$) o'zining yuqori dielektrik doimiysi tufayli metall–dielektrik–yarimo'tkazgich (MDY) tuzilmalar uchun istiqbolli material sifatida qaraladi. Biroq $TiO_2$ qatlamining kremniy taglik bilan bevosita kontakti interfeys holatlari zichligining ortishiga, oqish tokining ko'payishiga va sig'im–kuchlanish (C–V) xarakteristikalarida gisterezis paydo bo'lishiga olib keladi. Ushbu ishda kremniy taglik bilan $TiO_2$ dielektrik qatlami orasiga yupqa kremniy dioksid ($SiO_2$) oraliq qatlamini kiritish orqali interfeys sifatini yaxshilash masalasi ko'rib chiqilgan. Taklif etilgan $Si/SiO_2/TiO_2$/metall tuzilmasi doirasida oraliq qatlamning zaryad tutish markazlari zichligi (Dit), oqish toki va elektrofizik xossalarga ta'siri tahlil qilingan.*

***Kalit so'zlar:*** *MOS kondensator, titan dioksid ($TiO_2$), kremniy dioksid ($SiO_2$), oraliq qatlam, interfeys holatlari, zaryad tutish markazlari, oqish toki, sig'im–kuchlanish xarakteristikalari, gisterezis, dielektrik qatlam.*

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## ВЛИЯНИЕ ПРОМЕЖУТОЧНОГО СЛОЯ $SiO_2$ НА ЗАХВАТ ЗАРЯДА И ТОК УТЕЧКИ В СТРУКТУРАХ ПОЛУПРОВОДНИК–ДИЭЛЕКТРИК

***Аннотация.*** *Непрерывное масштабирование полупроводниковых приборов требует использования материалов с высокой диэлектрической проницаемостью. В связи с этим диоксид титана ($TiO_2$) благодаря высокой диэлектрической постоянной рассматривается как перспективный материал для структур металл–диэлектрик–полупроводник (МДП). Однако непосредственный контакт слоя $TiO_2$ с кремниевой подложкой приводит к увеличению плотности поверхностных состояний, росту тока утечки и появлению гистерезиса на вольт-фарадных (C–V) характеристиках. В данной работе рассмотрено улучшение качества границы раздела путём введения тонкого промежуточного слоя диоксида кремния ($SiO_2$) между кремниевой подложкой и диэлектрическим слоем $TiO_2$. В рамках предложенной структуры $Si/SiO_2/TiO_2$/металл теоретически проанализировано влияние промежуточного слоя на плотность центров захвата заряда (Dit), ток утечки и электрофизические свойства.*

***Ключевые слова:*** *MOS-конденсатор, диоксид титана ($TiO_2$), диоксид кремния ($SiO_2$), промежуточный слой, поверхностные состояния, центры захвата заряда, ток утечки, вольт-фарадные характеристики, гистерезис, диэлектрический слой.*

**Introduction.** The rapid development of modern micro- and nanoelectronics requires a significant reduction in the dimensions of semiconductor devices as well as an improvement in their electrical performance. This, in turn, increases the requirements for the properties of dielectric materials used in metal–dielectric–semiconductor (MDS) structures. Although silicon dioxide ($SiO_2$) has been widely used as a dielectric layer, its low dielectric permittivity limits its ability to provide high capacitance values [1,5]. For this reason, in recent years, materials with high dielectric permittivity, including titanium dioxide ($TiO_2$), have been extensively studied as dielectric layers in MDS structures. $TiO_2$ is characterized by a high dielectric constant, a wide bandgap, and technological compatibility. These properties make it a promising material for the development of high-capacitance and miniaturized devices [2]. However, one of the main

problems in $TiO_2$-based MDS structures is the formation of a large number of defects and charge trapping centers at the interface between the titanium dioxide layer and the silicon substrate. These interface defects lead to stretching of the capacitance–voltage (C–V) characteristics, the appearance of hysteresis, and an increase in leakage current density. As a result, the electrical stability and reliability of the device are degraded [3].

**Methods.** In this study, a multilayer metal–dielectric–semiconductor structure consisting of a silicon substrate, a thin silicon dioxide ($SiO_2$) interfacial layer, a titanium dioxide ($TiO_2$) main dielectric layer, and a metal electrode is proposed. The proposed structure is represented as follows: Al/$TiO_2$/$SiO_2$/Si. In this structure, the $SiO_2$ interfacial layer serves to improve the interface quality between the semiconductor and the high-k dielectric layer [4]. The semiconductor substrate is n-type doped silicon (Si), which serves as the medium where charge carriers are redistributed. The interfacial layer is silicon dioxide ($SiO_2$) with a thickness of 0.5–3 nm, which is used for interface passivation. The main dielectric layer is titanium dioxide ($TiO_2$) with a thickness of 10–25 nm, which provides high capacitance due to its high dielectric permittivity. The metal electrode (Al) is used to apply external voltage and generate an electric field. The key feature of the proposed structure is the presence of the $SiO_2$ interfacial layer, which eliminates the direct contact between $TiO_2$ and silicon and reduces interface defects.

The fabrication of the metal–dielectric–semiconductor structure is carried out through the following technological steps. First, the surface of the n-type silicon wafer is cleaned from organic and inorganic contaminants. Then, the native oxide layer is removed by short-term treatment in a diluted HF solution. This step is important to ensure surface cleanliness and the formation of high-quality subsequent layers.

A thin $SiO_2$ layer with a thickness of 0.5–3 nm is formed on the silicon surface. This layer is produced by thermal oxidation or other suitable technological methods. The thickness of the layer is controlled using spectroscopic ellipsometry. A $TiO_2$ dielectric layer with a thickness of 10–25 nm is deposited on top of the $SiO_2$ layer using atomic layer deposition (ALD). This method allows precise control of the layer thickness and ensures the formation of a uniform and high-quality film. A metal electrode (Al) is deposited on top of the $TiO_2$ layer using physical vapor deposition (PVD). The metal layer serves to transmit the external electrical signal. The fabricated structure is then subjected to thermal annealing at a temperature of 300–400°C in a nitrogen ambient. This process improves the interface quality, reduces defects, and stabilizes the electrical properties of the dielectric layer.

**Results and Discussion.** In metal–dielectric–semiconductor (MDS) structures, the presence of defects leads to the stretching of the C–V curve, a slow variation of capacitance with voltage, and the appearance of hysteresis (difference between forward and reverse sweeps). The hysteresis phenomenon is explained by the trapping of charges and their asymmetric redistribution. When an $SiO_2$ interfacial layer is introduced, the density of interface states decreases, charge exchange becomes faster, and the C–V characteristics approach the ideal behavior. As a result, the electrical stability of the device improves. Fig.1(a) shows the C–V characteristic for the Si/$TiO_2$ structure without an interfacial layer. In this case, a significant stretching of the curve is observed, which is explained by a high density of interface states ($D_{it}$). The trapping and delayed release of charge carriers through interface states lead to non-ideal C–V characteristics. Fig.1(b) presents the C–V characteristic for the Si/$SiO_2$/$TiO_2$ structure with an interfacial layer. In this case, the curve becomes steeper, indicating a reduction in the density of interface states. In addition, a voltage shift of the C–V characteristic is observed, which is related to surface charges and the redistribution of the internal electric field. At the same time, a slight decrease in the maximum capacitance is explained by the presence of the additional $SiO_2$ dielectric layer.

In MOS capacitors, leakage current arises due to the transport of charge carriers through the dielectric layer. This process can occur via several physical mechanisms. In $TiO_2$-based structures, the following mechanisms are dominant: direct tunneling, in which charge carriers pass through the energy barrier in thin dielectric layers; Fowler–Nordheim tunneling, which occurs under a strong electric field when charge carriers tunnel through a potential barrier; and Poole–Frenkel emission, which is associated with defects in the dielectric, where charge carriers are released from trap centers under the influence of an electric field and contribute to conduction. Due to the high density of defects in $TiO_2$, trap-assisted conduction plays a dominant role. The introduction of an $SiO_2$ interfacial layer increases the energy barrier height, reduces the number of defects, and interrupts conduction paths. As a result, the leakage current is significantly reduced. Fig.1(c) shows the comparison of I–V characteristics. It can be seen that the leakage current density is significantly lower in the presence of the $SiO_2$ interfacial layer. This is explained by the increase in the energy barrier and the suppression of defect-assisted conduction mechanisms.

In metal–dielectric–semiconductor structures, the interface between the dielectric layer and the semiconductor is a key factor determining the electrophysical properties of the device. Ideally, this interface should be perfect; however, in practice, defects arise due to broken atomic bonds, lattice imperfections, and chemical mismatches. These defects act as charge trapping centers, which can temporarily capture charges through energy states within the bandgap. The density of these centers is expressed as the interface state density ($D_{it}$). In the case of direct contact between $TiO_2$ and silicon, the $D_{it}$ value is high, leading to charge trapping and delayed release, stretching of the C–V characteristics, hysteresis, and temporal instability of device parameters. The introduction of an $SiO_2$ interfacial layer significantly reduces interface defects by passivating dangling bonds on the silicon surface. As a result, the Dit value decreases and charge trapping is suppressed. Fig.1(d) shows the energy distribution of the interface state density (Dit). It is observed that the Dit values decrease over the entire energy range when the $SiO_2$ interfacial layer is introduced. This is attributed to the passivation of the silicon surface and the reduction of dangling bonds.

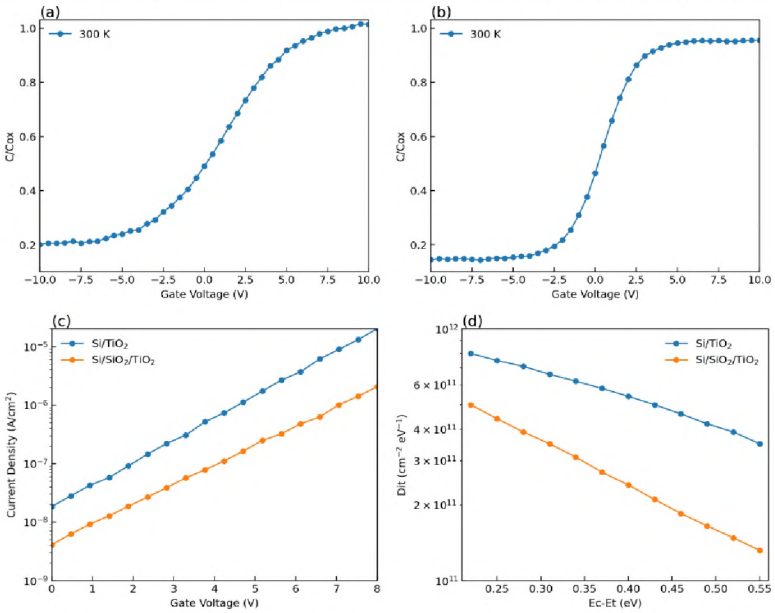



**Fig.1. Electrophysical characteristics of $Si/TiO_2$ and $Si/SiO_2/TiO_2$ MDS structures.**

The thickness of the $SiO_2$ interfacial layer has a significant effect on the main parameters of the device. In the case of a very thin layer (<0.5 nm), sufficient passivation is not achieved and defects remain. An optimal thickness (1–2 nm) provides maximum interface passivation and reduces Dit. In contrast, for a thick layer (>3 nm), the total dielectric thickness increases and the capacitance decreases. Therefore, by optimizing the $SiO_2$ thickness, a balance between capacitance and electrical stability can be achieved. The electrophysical properties of the proposed $Si/SiO_2/TiO_2$/metal MOS structure were analyzed, and the effect of the $SiO_2$ interfacial layer on device performance was evaluated.

The hysteresis phenomenon arises due to the trapping of charges in the dielectric layer or at the interface and their delayed release. In $TiO_2$-based structures, hysteresis is pronounced due to the high $D_{it}$ value, the large number of defect centers, and the trapping of charges in these centers. The $SiO_2$ interfacial layer passivates the interface, reduces the number of charge trapping centers, and accelerates charge exchange processes. As a result, hysteresis is significantly reduced and the switching characteristics of the device are improved.

**Conclusion.** The possibility of improving the interface properties in $TiO_2$-based metal–dielectric–semiconductor (MOS) capacitors by introducing a thin $SiO_2$ interfacial layer between the silicon substrate and the dielectric layer was analyzed. The analysis shows that the direct contact between $TiO_2$ and silicon leads to the formation of a high density of interface states, which results in an increase in leakage current, the appearance of hysteresis in capacitance–voltage (C–V) characteristics, and a degradation of device stability.

The introduction of the $SiO_2$ interfacial layer reduces these defects by passivating the silicon surface and suppresses charge trapping processes. As a result, the following improvements are expected for the proposed $Si/SiO_2/TiO_2$ structure:

reduction of leakage current density; decrease in interface state density; stabilization of capacitance–voltage characteristics; significant reduction of hysteresis.

In addition, it was shown that the optimization of the $SiO_2$ interfacial layer thickness plays an important role in achieving a balance between capacitance and electrical stability of the device. According to theoretical analysis, the optimal thickness is in the range of 1–2 nm.

**References:**

(1). Robertson J. High dielectric constant oxides. European Physical Journal Applied Physics, 28(3), p. 265–291.

(2). Wilk G.D., Wallace R.M., Anthony J.M. High-k gate dielectrics: Current status and materials properties considerations. Journal of Applied Physics, 89(10), p. 5243–5275.

(3). Sze S.M., Ng K.K. Physics of Semiconductor Devices. Wiley-Interscience.

(4). Houssa M. High-k Gate Dielectrics. Institute of Physics Publishing.

(5). Kingon A.I., Maria J.P., Streiffer S.K. Alternative dielectrics to silicon dioxide for memory and logic devices. Nature, 406, p. 1032–1038.

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## INFLUENCE OF SELF-HEATING ON ELECTRICAL PERFORMANCE OF Si/GaAs HETEROJUNCTIONS

***Annotation.*** *This study presents an analytical and numerical investigation of self-heating effects on the electrical performance of Si/GaAs heterojunctions. The thermal conductivities of silicon (150 W/m·K) and gallium arsenide (55 W/m·K) are considered along with key parameters such as current density ($10^4$–$10^5$ A/cm²) and electric field ($2\times10^5$–$5\times10^5$ V/cm). A coupled electrothermal model is used to evaluate temperature rise and its impact on device characteristics. The results show that the device temperature increases from 300 K to approximately 360–420 K under high current conditions. As a result, carrier mobility decreases by 25–35%, while leakage current increases by up to 2–3 times. The output current is reduced by approximately 15–20% due to thermal effects. Analytical calculations are in good agreement with numerical simulations, confirming that self-heating significantly affects carrier transport and device performance. These results emphasize the importance of thermal management in Si/GaAs heterojunction devices.*

***Keywords:*** *Si/GaAs heterojunction, self-heating, thermal conductivity, electrothermal modeling, numerical analysis, carrier mobility*

## Si/GaAs GETEROOTISHLARIDA O‘Z-O‘ZIDAN QIZISHNING ELEKTR XUSUSIYATLARIGA TA’SIRI

***Annotatsiya.*** *Ushbu ishda Si/GaAs geterootishlarida o‘z-o‘zidan qizishning elektr xususiyatlariga ta’siri analitik va sonli usullar yordamida o‘rganildi. Kremniy (150 W/m·K) va galliy arsenid (55 W/m·K) issiqlik o‘tkazuvchanligi, shuningdek, tok zichligi ($10^4$–$10^5$ A/cm²) va elektr maydon kuchlanganligi ($2\times10^5$–$5\times10^5$ V/cm) hisobga olindi. Bog‘langan elektroissiqlik modeli asosida harorat oshishi va uning qurilma xususiyatlariga ta’siri baholandi. Natijalar shuni ko‘rsatadiki, yuqori tok zichliklarida qurilma harorati 300 K dan 360–420 K gacha oshadi. Natijada tashuvchilar harakatchanligi 25–35%ga kamayadi, oqish toklar esa 2–3 baravar ortadi. Issiqlik ta’siri sabab chiqish toki taxminan 15–20%ga kamayadi. Analitik hisoblashlar sonli modellashtirish natijalari bilan yaxshi mos keladi va o‘z-o‘zidan qizishning qurilma ishlashiga sezilarli ta’sirini tasdiqlaydi.*

***Kalit so‘zlar:*** *Si/GaAs geterootish, o‘z-o‘zidan qizish, issiqlik o‘tkazuvchanligi, elektro-issiqlik modellashtirish, sonli tahlil, tashuvchilar harakatchanligi*