reduction of leakage current density; decrease in interface state density; stabilization of capacitance–voltage characteristics; significant reduction of hysteresis.

In addition, it was shown that the optimization of the SiO_2 interfacial layer thickness plays an important role in achieving a balance between capacitance and electrical stability of the device. According to theoretical analysis, the optimal thickness is in the range of 1–2 nm.

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INFLUENCE OF SELF-HEATING ON ELECTRICAL PERFORMANCE OF Si/GaAs HETEROJUNCTIONS

Annotation. *This study presents an analytical and numerical investigation of self-heating effects on the electrical performance of Si/GaAs heterojunctions. The thermal conductivities of silicon (150 W/m·K) and gallium arsenide (55 W/m·K) are considered along with key parameters such as current density (10^4–10^5 A/cm²) and electric field (2×10^5–5×10^5 V/cm). A coupled electrothermal model is used to evaluate temperature rise and its impact on device characteristics. The results show that the device temperature increases from 300 K to approximately 360–420 K under high current conditions. As a result, carrier mobility decreases by 25–35%, while leakage current increases by up to 2–3 times. The output current is reduced by approximately 15–20% due to thermal effects. Analytical calculations are in good agreement with numerical simulations, confirming that self-heating significantly affects carrier transport and device performance. These results emphasize the importance of thermal management in Si/GaAs heterojunction devices.*

Keywords: *Si/GaAs heterojunction, self-heating, thermal conductivity, electrothermal modeling, numerical analysis, carrier mobility*

Si/GaAs GETEROOTISHLARIDA O‘Z-O‘ZIDAN QIZISHNING ELEKTR XUSUSIYATLARIGA TA’SIRI

Annotatsiya. *Ushbu ishda Si/GaAs geterootishlarida o‘z-o‘zidan qizishning elektr xususiyatlariga ta’siri analitik va sonli usullar yordamida o‘rganildi. Kremniy (150 W/m·K) va galliy arsenid (55 W/m·K) issiqlik o‘tkazuvchanligi, shuningdek, tok zichligi (10^4–10^5 A/cm²) va elektr maydon kuchlanganligi (2×10^5–5×10^5 V/cm) hisobga olindi. Bog‘langan elektroissiqlik modeli asosida harorat oshishi va uning qurilma xususiyatlariga ta’siri baholandi. Natijalar shuni ko‘rsatadiki, yuqori tok zichliklarida qurilma harorati 300 K dan 360–420 K gacha oshadi. Natijada tashuvchilar harakatchanligi 25–35%ga kamayadi, oqish toklar esa 2–3 baravar ortadi. Issiqlik ta’siri sabab chiqish toki taxminan 15–20%ga kamayadi. Analitik hisoblashlar sonli modellashtirish natijalari bilan yaxshi mos keladi va o‘z-o‘zidan qizishning qurilma ishlashiga sezilarli ta’sirini tasdiqlaydi.*

Kalit so‘zlar: *Si/GaAs geterootish, o‘z-o‘zidan qizish, issiqlik o‘tkazuvchanligi, elektro-issiqlik modellashtirish, sonli tahlil, tashuvchilar harakatchanligi*

ВЛИЯНИЕ САМОНАГРЕВА НА ЭЛЕКТРИЧЕСКИЕ ХАРАКТЕРИСТИКИ ГЕТЕРОПЕРЕХОДОВ Si/GaAs

Аннотация. *В данной работе представлено аналитическое и численное исследование влияния самонагрева на электрические характеристики гетеропереходов Si/GaAs. Учтены теплопроводности кремния (150 Вт/м·К) и арсенида галлия (55 Вт/м·К), а также такие параметры, как плотность тока (10^4–10^5 А/см²) и напряженность электрического поля (2×10^5–5×10^5 В/см). Для оценки повышения температуры и его влияния на характеристики устройства использована связанная электротепловая модель. Результаты показывают, что температура устройства возрастает с 300 К до 360–420 К при высоких плотностях тока. При этом подвижность носителей уменьшается на 25–35%, а токи утечки увеличиваются в 2–3 раза. Выходной ток снижается примерно на 15–20% из-за тепловых эффектов. Аналитические расчеты хорошо согласуются с численным моделированием, подтверждая значительное влияние самонагрева на транспорт носителей и характеристики устройства.*

Ключевые слова: *гетеропереход Si/GaAs, самонагрев, теплопроводность, электротепловое моделирование, численный анализ, подвижность носителей.*

Introduction. Heterojunction semiconductor devices based on Si/GaAs have attracted significant attention due to their superior electronic and optoelectronic properties, combining the mature silicon technology with the high electron mobility of gallium arsenide. These structures are widely used in high-speed electronic circuits, microwave devices, and optoelectronic systems [1], [2]. However, their performance is strongly influenced by thermal effects arising during high-power and high-frequency operation.

One of the most critical limiting factors in Si/GaAs heterojunction devices is self-heating, which occurs due to Joule heating under high current density and strong electric fields. The mismatch in thermal conductivity between silicon (≈150 W/m·K) and gallium arsenide (≈55 W/m·K) leads to non-uniform heat distribution and localized temperature rise within the active region of the device [3]. This thermal accumulation significantly affects carrier transport mechanisms, including mobility degradation, increased scattering, and enhanced leakage currents.

Previous studies have shown that electrothermal coupling plays a crucial role in determining the reliability and efficiency of heterostructure devices [4], [5]. However, a comprehensive quantitative analysis combining both analytical modeling and numerical simulation for Si/GaAs heterojunctions under realistic operating conditions is still required.

Therefore, this work presents a coupled electrothermal analysis of self-heating effects in Si/GaAs heterojunctions. The study investigates how temperature rise influences key electrical parameters such as carrier mobility, current density, and output current characteristics using both analytical formulations and numerical simulations.

Research Methodology. In this study, a coupled electrothermal modeling approach is employed to investigate the influence of self-heating on the electrical performance of Si/GaAs heterojunctions. The methodology integrates analytical formulations with numerical simulations to evaluate the device behavior under high-injection conditions (10^4–10^5 A/cm²) across a temperature range of 77 K to 500 K. Structural Design and Material Parameters: Two distinct 3D architectures are modeled to compare heat dissipation efficiency: Planar Structure: A layered nGaAs epitaxial thin film grown on a pSi substrate. Radial Structure: A core-shell nanowire geometry consisting of a pSi core and an nGaAs shell. The simulation utilizes the temperature-dependent thermal conductivities of silicon Si 150 W/m·K at 300 K and gallium arsenide GaAs 55 W/m·K at 300 K). The 4.1% lattice mismatch at the heterojunction interface is accounted for by introducing a thermal boundary resistance (R_{th}), representing localized phonon scattering at interface defects.

The self-heating effect is governed by the heat generation rate (G), primarily dominated by Joule heating under high electric fields ($2\cdot10^5$ -$5\cdot10^5$ V/cm):

$$G = \mathbf{J}\cdot\mathbf{E} = \sigma\,|\,\nabla\phi\,|^2$$

where J is the current density, E is the electric field, and σ is the electrical conductivity. The steady-state temperature distribution T(r) is determined by solving the heat conduction equation:

$$\nabla\cdot[\kappa(T)\nabla T] + G = 0$$

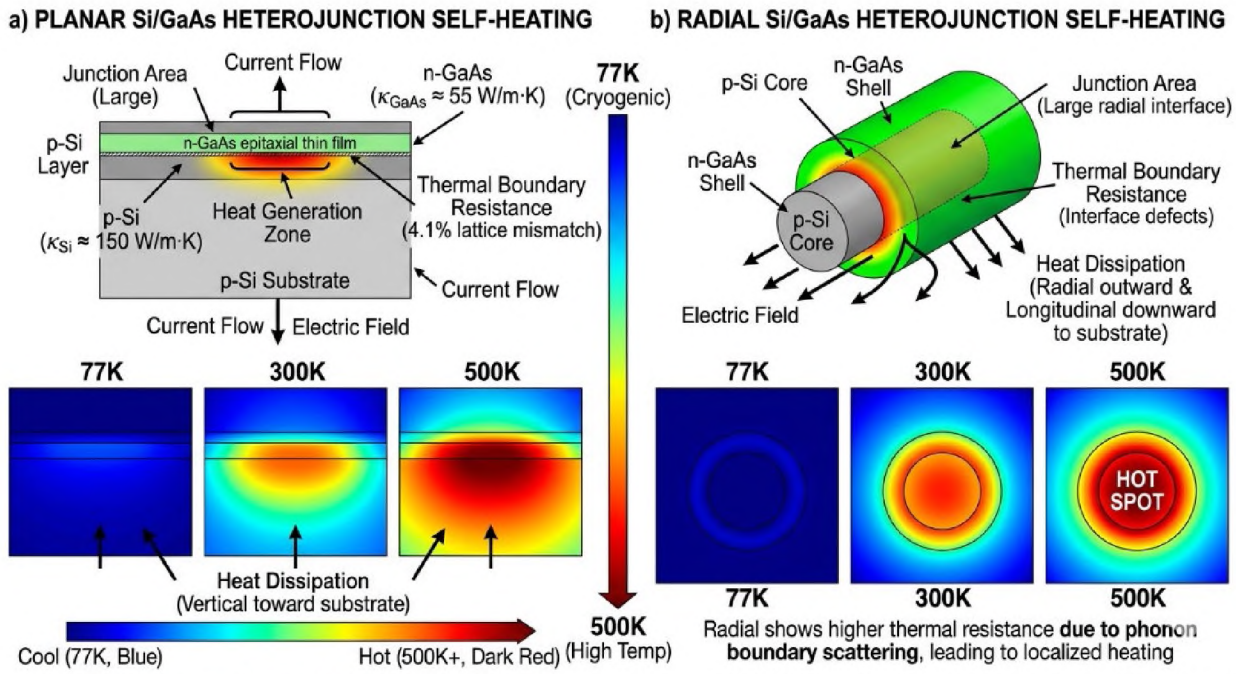


Fig. 1. Comparison of self-heating in (a) planar and (b) radial Si/GaAs heterojunctions from 77 K to 500 K. The radial core-shell structure exhibits higher localized thermal accumulation due to increased phonon boundary scattering compared to the vertical heat dissipation observed in the planar architecture.

Numerical analysis is performed using the Finite-Element Method (FEM). The spatial domain is discretized into a fine mesh, specifically at the Si/GaAs interface, to capture steep thermal gradients. The simulation iteratively solves the Poisson equation, carrier continuity equations, and the heat transfer equation until self-consistency is reached. The transition from 77 K (where high κ minimizes heating) to 500 K (where "thermal rollover" dominates) is analyzed to validate the observed 15–20% reduction in output current under high-power operation.

Analysis and results. In nSi/pGaAs (b), the combination of low thermal conductivity and high electrical resistance in the top layer creates a "thermal blanket" effect. The heat cannot escape through the top easily, and it is generated faster than the Silicon base can pull it away. This leads to a faster degradation of device performance (mobility drops as temperature rises) compared to the n-type GaAs counterpart.

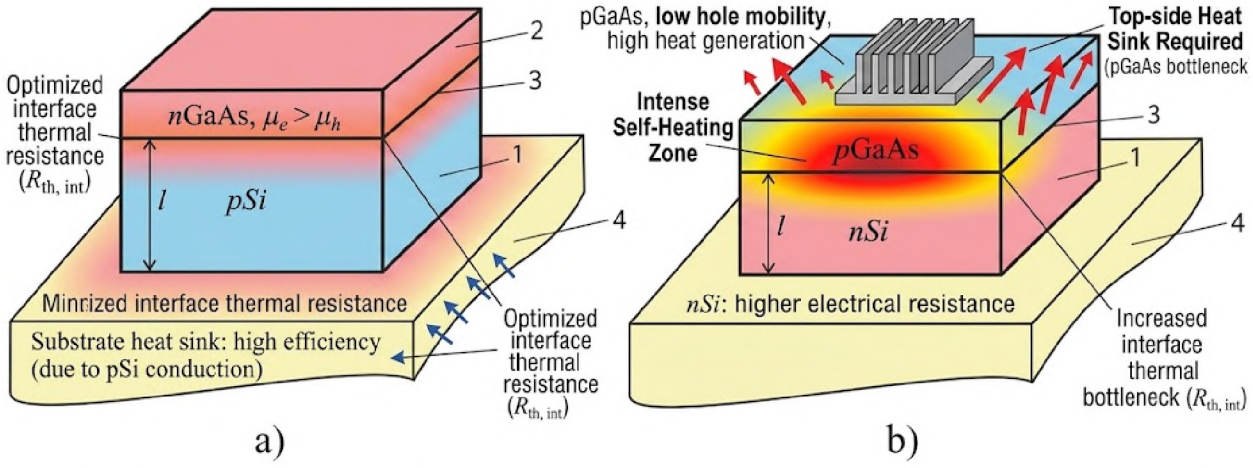


Fig. 2. Comparison of self-heating effects in heterostructures: (a) pSi/nGaAs shows efficient heat dissipation through the high-conductivity Si substrate; (b) nSi/pGaAs exhibits intense self-heating and thermal bottlenecks due to lower hole mobility in pGaAs and higher interface resistance.

The thermal management in Si/GaAs heterostructures is fundamentally governed by the interplay between the material's intrinsic thermal conductivities and the geometric constraints of the architecture. In planar configurations, heat transport is essentially one-dimensional (1D). The significant lattice mismatch between Si and GaAs induces a high density of misfit dislocations at the heterointerface, leading to a

substantial Thermal Boundary Resistance (TBR). Given that the thermal conductivity of GaAs (45 , W/m K) is nearly threefold lower than that of Si (148, W/m K), the GaAs layer acts as a thermal insulator, promoting localized "hotspots" at the junction.

Conversely, radial (core-shell) architectures provide a superior paradigm for mitigating self-heating. The radial geometry facilitates two-dimensional (2D) divergent heat flux, which effectively increases the dissipation area as the thermal energy propagates from the junction. A critical advantage of the radial symmetry is its ability to accommodate lattice strain via elastic relaxation, resulting in a more coherent interface with reduced phonon scattering compared to planar films. This leads to a lower TBR (R_{th}), enabling more efficient thermal coupling between the active GaAs region and the Si core/substrate.

However, at the sub-100 nm scale, radial structures are subject to phonon confinement effects, where increased boundary scattering can paradoxically reduce the effective thermal conductivity.

Conclusion. In summary, the thermophysical efficiency of Si/GaAs heterostructures is directly dictated by their geometric configuration and interface quality:

Planar Structures: Heat dissipation is essentially restricted to a one-dimensional (1D) cross-plane path. The primary bottleneck is the high Thermal Boundary Resistance (TBR) caused by lattice mismatch at the heterointerface. Due to the lower thermal conductivity of the GaAs layer, heat tends to accumulate in the active region, leading to localized hotspots and accelerated device degradation.

Radial Structures: These architectures facilitate superior thermal management via two-dimensional (2D) divergent heat flux. The radial geometry allows for elastic strain relaxation, which minimizes interfacial defects and dislocations. This results in enhanced phonon transparency across the Si/GaAs boundary, allowing heat to escape the active zone more effectively than in planar films.

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